WHAT IS CLAIMED IS:

1. A method for designing a semiconductor device comprising;

receiving a net list of a semiconductor device;

temporarily locating a plurality of functional blocks within a layout area of the semiconductor device;

dividing a logic area of the semiconductor device into a plurality of rectangular areas;

computing a predicted value of a utilization rate of the logic area and a predicted value of a wiring length of the semiconductor device based on a data base regarding a semiconductor device designed previously and the semiconductor device and the net list of the semiconductor device;

locating, dividing and computing when the predicted value of the utilization rate of the logic area of the semiconductor device does not satisfy a predetermined condition;

outputting floor plan information for allocating the plurality of functional blocks basic cells and wiring within the logic area of the semiconductor device when the predicted value of the utilization rate of the logic area satisfies the predetermined condition; and

outputting the predicted value of the wiring length of the semiconductor device.

2. The method of designing a semiconductor device claimed in claim 1 further comprising:

producing the data base including information regarding a basic cell located in a logic area of the semiconductor device designed previously, information regarding a net list of the semiconductor device designed previously, information regarding a wiring length of the semiconductor device designed

previously, information regarding a utilization rate of the logic area of the semiconductor device designed previously, or information regarding the basic cell possibly located in the logic area of the semiconductor device.

3. The method of designing a semiconductor device claimed in claim 2, wherein, the information regarding the basic cell located in the logic area of the semiconductor device designed previously or the information regarding the basic cell possibly located in the logic area of the semiconductor device includes information regarding a number of pins held by the basic cell, information regarding a number of nets connected to the basic cell or information regarding a kind of basic cell.

4. The method of designing a semiconductor device claimed in claim 2, wherein the information regarding the basic cell located in the logic area of the semiconductor device designed previously includes a total number of gates, information regarding a relationship between the net list and the number of pins, which is obtained by classifying all nets in terms of a connection pin number.

5 The method of designing a semiconductor device claimed in claim 2, wherein, information regarding the wiring length of the semiconductor device designed previously includes information regarding a total wiring length of the net list when a number of layers of aluminum wiring layers are predetermined or information regarding a relationship between a number of pins and wiring length, obtained by classifying all nets in terms of a connection pin number.

6. The method of designing a semiconductor device claimed in claim 2, wherein information regarding the utilization rate of the logic area of the

semiconductor device designed previously includes a maximum value of the utilization rate in case when a number of layers of aluminum wiring layers is a predetermined number and a configuration of the logic area is a square.

7. The method of designing a semiconductor device claimed in claim 2 further comprising:

producing a first equation for computing a predicted value of an average value of the wiring length of a total number of nets for the semiconductor device a second equation for computing a gradient in a graph where a number of connecting pins is along the abscissa and a predicted value of an average value of the wiring length of a net for every number of connecting pins along the ordinate, or a third equation for computing a predicted value of an average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", based on the data base, in response to a number of layers of aluminum wiring layers of the semiconductor device;

using the first to the third equations and the net list of the semiconductor device and computing; the predicted value of an average value of the wiring length of the total number of nets of the semiconductor device; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of a net for every number of connecting pins along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of a net of which the number of connecting pins within the net of the semiconductor device is two "2", in response to the number of layers of aluminum wiring layers of the semiconductor device;

a step (j) correcting; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor; the gradient in

the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins along the ordinate with respect to the total nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", that were computed in the step(i), in response to the configuration of the rectangular area,

a step (k) producing a fourth equation for computing the predicted value of the utilization rate of the logic area of the semiconductor device based on;

the data base;

the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device;

the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins along the ordinate with respect to the total number of nets of the semiconductor device;

or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", that were computed in the step(i); and

the total number of nets of the semiconductor device in response to the number of layers of aluminum wiring layers of the semiconductor device;

a step (l) computing the predicted value of the utilization rate of the logic area of the semiconductor device based on the fourth equation, in response to the number of layers of aluminum wiring layers of the semiconductor device; and

a step (m) correcting the predicted value of the utilization rate of the logic area of the semiconductor device in response to the configuration of the rectangular area.

8. The method of designing a semiconductor device claimed in claim 7, further comprising producing the first to third equations by a regression analysis producing and the fourth equation by the regression analysis.

9. The semiconductor device having been designed by the method of designing a semiconductor device claimed in claim 1.

10. An apparatus for designing a semiconductor device comprising:

means for inputting a net list of a semiconductor device and information that designates an arranged location of a plurality of functional blocks, which are located within the semiconductor device;

means for recording the net list of the semiconductor device;

means for recording a data base with respect to a semiconductor device designed previously and the semiconductor device;

means for recording information with respect to a basic cell located within the semiconductor device designed previously and the basic cell possibly located in a logic area of the semiconductor device;

means for temporarily arranging the plurality of functional blocks, which temporarily arranges the plurality of functional blocks within a layout region of the semiconductor device, in response to information designating the arranged location;

means for dividing the logic area of a semiconductor device into a plurality of rectangular areas;

means for computing a predicted value of a utilization rate of the logic area, which computes a predicted value of a wiring length and the predicted value of the utilization rate of the logic area of the semiconductor device based on the data base and the net list of the semiconductor device;

a means for judging the predicted value of the utilization rate of the logic area, which judges whether the predicted value of the utilization rate of the logic area in the semiconductor device satisfies a predetermined condition or not, and promoting a user to input information designating new arranged location for the plurality of functional blocks located within the semiconductor device when the predicted value of the utilization rate of the logic area does not satisfies the predetermined condition;

means for outputting floor plan information, which outputs floor plan information for arranging the plurality of functional blocks, basic cells, and wiring within the logic area of the semiconductor device or arranges the plurality of functional blocks, basic cells, and wiring when the predicted value of the utilization rate of the logic area satisfies the predetermined condition;

means for outputting the predicted value of the wiring length, which outputs the predicted value of the wiring length of the semiconductor device; and

means for displaying the layout of the semiconductor device where the plurality of functional blocks is temporarily arranged by the means for temporarily arranging a plurality of functional blocks an image for promoting the user to input information designating new arranged location for the plurality of functional blocks located within the semiconductor device when the predicted value of the utilization rate of the logic area does not satisfy the predetermined condition; and/or the layout of the semiconductor device where the plurality of functional blocks, basic cells, and wiring are arranged by the means for outputting floor plan information.

11. The apparatus for designing a semiconductor device claimed in claim 10 further comprising:

means for recording a net list of a semiconductor device designed

previously; and

means for producing the data base including information regarding a basic cell located within a logic area of a semiconductor device designed previously, information regarding the net list of the semiconductor device designed previously, information regarding a wiring length of the semiconductor device designed previously, information regarding a utilization rate of a logic area of the semiconductor device designed previously, and/or information regarding the basic cell to probably be arranged within the logic area of the semiconductor device based on the net list of the semiconductor device designed previously, information regarding the basic cell located within the logic area of the semiconductor device designed previously and the basic cell to probably be arranged within the logic area of the semiconductor device.

12. The apparatus for designing a semiconductor device claimed in claim 11, wherein the information regarding the basic cell located within the logic area of the semiconductor device designed previously or the information regarding a basic cell to probably be arranged within a logic area of the semiconductor device includes information regarding a numbers of pins included in the basic cell, information regarding a number of nets connected to the basic cell or information regarding a kind of basic cell.

13. The apparatus for designing a semiconductor device claimed in claim 11, wherein the information regarding the net list of the semiconductor device designed previously includes a total number of gates, information regarding a relationship between a number of pins and the net list, obtained by classifying all nets in terms of a connection pin number or information regarding a ratio of the number of nets to the number of pins.

14. The apparatus for designing a semiconductor device claimed in claim 11, wherein the information regarding the wiring length of the semiconductor device designed previously includes information regarding a total wiring length of the net list when a number of layers of aluminum wiring layers is a predetermined number or information regarding a relationship between the wiring length and a number of pins obtained by classifying all nets in terms of a connection pin number.

15. The apparatus for designing a semiconductor device claimed in claim 11, wherein the information regarding the utilization rate of the logic area of the semiconductor device designed previously includes a maximum value of the utilization rate when a number of layers of aluminum wiring layers is a predetermined number and a configuration of the logic area is a square.

16. The apparatus for designing a semiconductor device claimed in claim 11,wherein the means for computing the predicted value of the utilization rate of the logic area includes:

a unit for producing equations of the predicted value of an average value of the wiring length and others that produce; a first equation for computing a predicted value of an average value of a wiring length of a total number of nets for the semiconductor device; a second equation for computing a gradient in a graph where a number of connecting pins is along the abscissa and a predicted value of an average value of a wiring length of a net for every number of connecting pins along the ordinate; or a third equation for computing a predicted value of an average value of a wiring length of a net of which the number of connecting pins within the net of the semiconductor device is two "2", based on the data base, in response to number of layers of aluminum wiring layers of the semiconductor device;

a unit for computing the predicted value of the average value of the wiring length and others that uses the first to the third equations and the net list of the semiconductor device and computes; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of an average value of the wiring length of the net every for number of connecting pins along the ordinate with respect to the total nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", in response to the number of layers of aluminum wiring layers of the semiconductor device;

a first correcting unit that corrects; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", that were computed in the unit for computing the predicted value of the average value of the wiring length and others, in response to the configuration of the rectangular area,

a unit for producing an equation for computing the predicted value of the utilization rate that produces a fourth equation for computing the predicted value of the utilization rate of the logic area of the semiconductor device based on; the data base; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device; the gradient in the

graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", that were computed in the unit for computing the predicted value of the average value of the wiring length and others, and the net list of the semiconductor device in response to the number of layers of aluminum wiring layers of the semiconductor device;

a unit for computing the predicted value of the utilization rate that computes the predicted value of the utilization rate of the logic area of the semiconductor device based on the fourth equation, in response to the number of layers of aluminum wiring layers of the semiconductor device; and

a second correcting unit that corrects the predicted value of the utilization rate of the logic area of the semiconductor device in response to the configuration of the rectangular area.

17. The apparatus for designing a semiconductor device claimed in claim 16, wherein the unit for producing equations of the predicted value of the average value of the wiring length and others produces the first to third equations by a regression analysis and the unit for producing the equation for computing the predicted value of the utilization rate produces the fourth equation by the regression analysis.

18. A program of designing a semiconductor device, making a CPU execute:

a step (a) receiving a net list of a semiconductor device;

a step (b) temporarily locating a plurality of functional blocks within a

layout area of the semiconductor device;

a step (c) dividing a logic area of the semiconductor device, into a plurality of rectangular areas;

a step (d) computing a predicted value of a utilization rate of the logic area and a predicted value of a wiring length of the semiconductor device based on a data base regarding a semiconductor device designed previously and the semiconductor device and a net list of the semiconductor device;

a step (e) repeating the step (b) to the step (d) when the predicted value of the utilization rate of the logic area of the semiconductor device does not satisfy a predetermined condition;

a step (f) outputting floor plan information for allocating the plurality of functional blocks, basic cells and wiring within the logic area of the semiconductor device when the predicted value of the utilization rate of the logic area of the semiconductor device satisfies the predetermined condition; and

a step (g) outputting the predicted value of the wiring length of the semiconductor device.

19. The program of designing a semiconductor device claimed in claim 18, making a CPU execute a step for producing the data base including information regarding a basic cell located within a logic area of the semiconductor device designed previously, information regarding the net list of the semiconductor device designed previously, information regarding wiring length of a semiconductor device designed in the past, information regarding a utilization rate of the logic area of the semiconductor device designed previously, or information regarding a basic cell to probably be arranged within the logic area of the semiconductor device.

20. The program claimed in claim 19, wherein the information regarding the basic cell located within the logic area of the semiconductor device designed previously or the information regarding the basic cell to probably be arranged within the logic area of the semiconductor device_includes information regarding a number of pins included in the basic cell, information regarding a number of nets connected to basic cell or information regarding a kind of basic cell.

21. The program claimed in claim 19, wherein the information regarding the net list of the semiconductor device designed previously includes a total number of gates, information regarding a relationship between a number of pins and the net list obtained by classifying all nets in terms of a connection pin number or information regarding a ratio of a number of nets to the numbers of pins.

22. The program claimed in claim 19, wherein the information regarding the wiring length of the semiconductor device designed previously includes information regarding a total wiring length of the net list when a number of layers of aluminum wiring layers is a predetermined number or information regarding a relationship between the wiring length and a number of pins obtained by classifying all nets in terms of a connection pin number.

23. The program claimed in claim 20, wherein the information regarding the utilization rate of the logic area of the semiconductor device designed previously, includes a maximum value of a rate of the utilization when the number of layers of aluminum wiring layers is a predetermined number and a configuration of the logic area is a square.

24. The program claimed in claim 19, wherein step (d) includes:

a step (h) producing a first equation for computing a predicted value of an average value of a wiring length of a total number of nets for the semiconductor device, a second equation for computing a gradient in a graph where a number of connecting pins is along the abscissa and a predicted value of an average value of a wiring length of a net for every number of connecting pins along the ordinate or a third equation for computing a predicted value of an average value of a wiring length of a net of which a number of connecting pins within a net of the semiconductor device is two "2",based on the data base, in response to the number of layers of aluminum wiring layers of the semiconductor device;

a step (i) using the first to the third equations and the net list of the semiconductor device and computing, the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device the gradient of the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins is along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2", in response to the number of layers of aluminum wiring layers of the semiconductor device;

a step (j) correcting the predicted value of the average value of the wiring length of the total number of nets of the semiconductor device; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins is along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting

pins within the net of the semiconductor device is two "2", that were computed in the step(i), in response to the configuration of the rectangular area;

a step (k) producing a fourth equation for computing a predicted value of the utilization rate of the logic area of the semiconductor device based on; the data base; the predicted value of the average value of the wiring length of the total number of nets of the semiconductor; the gradient in the graph where the number of connecting pins is along the abscissa and the predicted value of the average value of the wiring length of the net for every number of connecting pins is along the ordinate with respect to the total number of nets of the semiconductor device; or the predicted value of the average value of the wiring length of the net of which the number of connecting pins within the net of the semiconductor device is two "2" that were computed in the step(i), and the total nets of the semiconductor device in response to the number of layers of aluminum wiring layers of the semiconductor device;

a step (l) computing the predicted value of the utilization rate of the logic area of the semiconductor device, based on the fourth equation, in response to the number of layers of aluminum wiring layers of the semiconductor device; and

a step (m) correcting the predicted value of the utilizations rate of the logic area of the semiconductor device in response to the configuration of the rectangular area.

25. The program claimed in claim 24, wherein step (h) produces the first to third equations by regression analysis and step (l) produces the fourth equation by regression analysis.